Remarks

1. **The Limitation "substantially conforming to the substrate surface contour" in Claims 1 and 13 is fully supported in the Specification.**

Responding to Office Action dated July 23, 2002, Applicants amended claims 1 and 13 to limit the insulation layer to conform substantially to the substrate surface contour. This limitation is fully supported in the description portion of the original specification, which goes on to explain that conformity means the insulation layer's surface is irregular and the irregularity imitates the topography of the underlying structure.[1] The original drawing figure 1C also evidences this conformity.

2. **The Lin reference teaches a corresponding but non-conformal layer.**

Examiner Perez correctly pointed out that layer 40 of the Lin reference corresponds to the insulation layer of the present invention. But the Lin reference specifically restricts this layer to be "non-conformal".[2] It goes so far as saying that an important difference between layer 40 and prior art CVD, SACVD, and thermal oxide layers is this layer's non-conformity. In fact, it is the film's non-conformity that enables the process to achieve its stated object. This is one example of Lin reference teaching away from the present invention.

---

[1] Original Specification, page 9, paragraph 2.
[2] See Lin reference, column 5, line 40.

3. **The conformal etch barrier layer in the Lin reference does not read on the planarization layer in the present invention.**

Examiner Perez is also correct in identifying in Office Actions dated December 29, 2001 and again in July 23, 2002 that the barrier layer 44 corresponds to the planarization layer element in claims 1 and 13. But it is less accurate to hold that two layers locate in similar positions must perform similar functions because here they do not.

a. **The layers appear different.**

The planarization layer in the present invention has a flat or planar top surface. In the present disclosure, the term "planarization" has its customary meaning, i.e. to make a surface's curvature zero.[3] On the other hand, the barrier layer in the Lin reference has a top surface that conforms to the contour of the underlying surface. As shown in Fig. 2 of the Lin reference, the top and the bottom surfaces of layer 44 are spaced apart by the layer thickness and the layer follows closely to the top surface contour of layer. In fact, the Lin refers to this layer as "the conformal etch barrier layer.[4] This is another example of the Lin reference teaching away from the present invention.

b. **The layers are of different composition.**

The preferred material for this conformal etch barrier is silicon nitride and the preferred

[3] See Planar, Webster's New World College Dictionary, 3rd edition.
[4] See Lin reference, Column 6, line 40.

thickness range is between 200 Å to 500Å.[5] On the other hand, the planarization layer in the exemplary embodiment of the present invent planarizes a surface contour that includes isolation trenches with a depth between 5,000Å and 7,000Å.[6] And the exemplary embodiment suggests a resist etch back material be spun on the substrate to achieve such a planarization effect.[7] This makes it clear that the material for a conformal etch barrier layer as taught in the Lin reference cannot resemble the material suitable for a layer that planarizes a substrate with trenches at its surface.

c. **The layers function differently.**

In addition, in both claims 1 and 13 of the present invention there is an element that limits the removing step so that the rate of removing planarization layer and the rate of removing the insulation layer are substantially the same. This limitation is absent in the Lin reference because the conformal etch barrier layer in the Lin reference serves a different function.

What is required of the etch barrier layer is that it masks the area covered by it from the etching agent that etches the underlying material through openings in this etch barrier layer. On the other hand, the present invention does not require the planarization layer to serve as a etch mask. Instead, the function of the layer is to

[5] See Id. Column 6, line 41.
[6] Original Specification, page 6, line 26.
[7] Id. Page 10, line 10.

provide a flat, layered structure at the top of the substrate. Besides the flat top, the two components of the layered structure, i.e. the planarization layer and the insulation layer must have the same etch rate during a subsequent etching process. Thus ensures that upon completion of the etch step the top surface of the substrate maintains substantially smooth as depicted in Figure 1D.

Because the conformal etch barrier layer and the planarization layer look different, they are of different composition, and they serve different functions, the former cannot be said to read on the later.

4. Conclusion.

a. The independent claims stand patentable because the combined references lack limiting elements.

In summary, the amended claims 1 and 13 with the limitation of "substantially conforming to the substrate surface contour" is fully supported in the original specification and in the original drawing figure. The Lin reference lacks the elements of a insulation layer that substantially conforming to the substrate surface contour and it lacks the element of a planarization layer. The Yeh reference teaches a process for plasma cleaning the interior surfaces of semiconductor process chambers, which bears no direct connection to the present invention. And it too lacks the above-mentioned elements. Claims 1 and 13, therefore, stand patentable over

the combination of the Lin reference and the Yeh reference.

b. **Dependent claims stand patentable.**

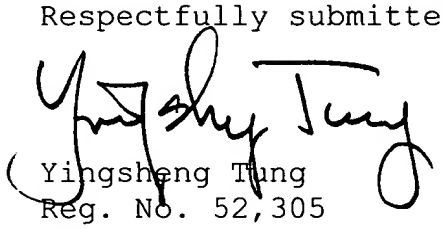
Claims 2-11 depend on claim 1 and include additional limitation not taught in the reference. Particularly, claim 2 further limits the of removing step to include etching through the planarization layer and the insulation layer down to a chemical mechanical polishing (CMP) depth and then chemical mechanically polishing it down to the polish stop layer. Claims 3 and 5 further limit the relative etch rates. Claim 4 further limits the etch to include a resist etch back plasma etch. Claim 6 further limits the removal of a polish stop layer. Claim 8 further limits the polish stop layer to include silicon nitride. Claim 9 further limits the insulation layer to include silicon oxide. Claim 11 further limits the CMP depth to be between 1,000 and 1,500 angstroms. Claims 2-12, therefore, stand patentable over the combination of the cited references.

Claims 14-20 depend on claim 13 and include further limitations not taught in the Lin reference. For the same reason as stated above, claims 14-20 also stand patentable over the combination of the cited references.

Applicants respectfully submit that the application is in allowable form and the claims distinguish over the cited

references. Applicants respectfully request the reconsideration or further examination of this application.

Respectfully submitted,



Yingsheng Tung
Reg. No. 52,305
Attorney for Applicants

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-5355